Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**7A**



**.019”**

**.027”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size:**

**Backside Potential:**

**Mask Ref: 7A**

**APPROVED BY: DK DIE SIZE .019” X .027” DATE: 4/20/23**

**MFG: LINEAR SYSTEMS THICKNESS .008” P/N: IT122**

**DG 10.1.2**

#### Rev B, 7/19/02